09-15-04

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Atty. Dkt. No. 039153-0223 (E0554)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yu

Title: MOS TRANSISTOR WITH ASYMMETRICAL SOURCE/DRAIN EXTENSIONS

Appl. No.: 09/476,961

Filing Date: 01/03/2000

Examiner: Warren, Matthew E.

Art Unit: 2815

CERTIFICATE OF EXPRESS MAILING

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EV 505795964 US (Express Mail Label Number)

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Jean M. Tibbetts (Printed Name)

Jean M. Tibbetts (Signature)

TRANSMITTAL OF REPLY BRIEF

Mail Stop – APPEAL BRIEF – PATENTS
Commissioner for Patents
P. O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Transmitted herewith are the following documents for the above-identified application.

[**X**] Reply Brief Under 37 C.F.R. § 1.193(b)(1) (5 pages, in triplicate).

[**X**] The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should non proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,

Date 9/14/04

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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REPLY BRIEF UNDER 37 C.F.R. § 1.193(b)(1)

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Sir:

In reply to the July 14, 2004 Examiner's Answer to the Appellant's Appeal Brief (hereinafter referred to as the "Examiner's Answer"), the following remarks are submitted in triplicate. These additional remarks include subject headings corresponding to the subject headings in the Examiner's Answer for ease of reference by the Board of Patent Appeals and Interferences.

(11) Response to Argument

(1) As indicated in the Appellant's Brief on Appeal dated January 27 (hereinafter referred to as the "Appeal Brief"), 2004, the Appellant submits that the combination of Kadosh and Miller does not teach or suggest the drain extension is deeper than the source extension limitation. In particular, Kadosh does not teach or suggest a drain extension deeper than a source extension (as indicated by the Examiner) and Miller does not

teach or suggest source and drain extensions or a drain extension deeper than a source extension.

In response to Appellant's arguments, the Examiner indicates that, as stated in prior arguments by the Examiner during prosecution, it is well known in the art that the source and drain are structurally the same. See, Examiner's Answer, page 6. The Examiner also states that applying opposite voltages to the structure in Figure 1N of Kadosh would result in source region 186 becoming a drain region and drain region 188 becoming a source region. See, Examiner's Answer, page 6. However, Appellant's submit, as discussed in prior responses during prosecution to the Examiner's argument, that the source and drain are distinct structures which have established meanings and functions. A drain is a region which contains a terminal into which charged carriers flow from the source through the channel and a source is a region which contains a terminal from which charged carriers flow toward the drain. Therefore, the source and drain are distinct structures that have distinct functions during the operation of the transistor. The invention as defined by independent claims 18, 21 and 31 is related to the specific functions of the source and drain and, therefore, the distinction between the source and drain cannot be ignored.

In the Examiner's Answer, the Examiner further states that Miller was cited to show that a drain extension is deeper than a source extension. See, Examiner's answer, page 6-page 7. In particular, the Examiner asserts that source underdiffusion length, U_s, and the drain underdiffusion length, U_d, as taught by Miller correspond and function as the source extension and the drain extension, respectively, taught in the present application. See, Examiner's Answer, page 7. However, Miller does not provide any discussion of a source extension or a drain extension or that drain underdiffusion length, U_d, and source underdiffusion length, U_s, function as an extension. In the present application, source extension 23 and drain extension 25 are regions disposed partially underneath a gate 18 and are used to, for example, help achieve immunity to short-channel effects which degrade transistor performance. See, Figure 1, Specification, page 1, lines 23-27, page 5, lines 18-23 and page 5, line 30- page 6, line 7. In particular, a shallower source extension and a deeper drain extension achieve at least three beneficial effects: 1) substantial immunity to short channel effects; 2) reduced peak electric field in the channel region reduces the possibility of

hot carrier injection into the gate oxide; and 3) higher drive current. See, Specification, page 3, lines 1-10.

In contrast, as discussed in the Appeal Brief, the drain and source underdiffusion lengths, U_d and U_s, are not of the same structure and function as the source and drain extensions of the present application. See, Appeal Brief, page 8. Rather, Miller teaches a drain underdiffusion length, U_d, and a source underdiffusion length, U_s, that are defined as the amount of overlap of gates 28 and drain region 27 and source regions 29, respectively. See, Miller, Figures 1 and 6, col. 1, lines 29-32 and lines 34-37 and col. 3, lines 57-62. A drain underdiffusion length, U_d, is provided that is longer than a source underdiffusion length, U_s, to achieve a desired gate-drain capacitance. See, Miller, Abstract, Figure 6, col. 2, lines 1-7, 15-19 and 26-31 and col. 3, lines 9-17 and lines 60-62. Alternatively, a source underdiffusion length may be provided that is longer than the drain underdiffusion length to achieve a desired gate-source capacitance. See, Miller, col. 4, lines 39-42. Accordingly, an increased gate–drain or gate-source capacitance is achieved without providing a separate gate-drain capacitor or gate-source capacitor and without requiring significant additional die area or critical mask alignment steps to form the capacitor. See, Miller, col. 1, lines 63-67. As shown in Figure 6 of Miller, the entire drain region 27 including the portion under the gate (as defined by the drain underdiffusion length) has the same diffusion depth. See, Miller, col. 3, lines 9-16. Appellant also notes that Miller does not even include a discussion of spacers used in conventional extension implant processes. Accordingly, Appellant's respectfully submit that Miller does not teach or suggest a source and drain extension.

In addition, in the Examiner's Answer, the Examiner states: "[f]urthermore, the gate length and asymmetrical underdiffusions of Miller improve the breakdown voltage characteristics of the silicon (col. 3, lines 57-67) therefore limiting the effects of the short channel or "hot carrier" effects (just as the Appellant's invention does)." See, Examiner's Answer, page 8. However, Appellant's respectfully submit that Miller does not teach that a longer underdiffusion length improves the breakdown voltage characteristics of the silicon therefore limiting the effects of the short channel or "hot carrier effects. In addition, Miller does not teach or suggest the functions of a source and drain extension or the benefits of a

structure having a drain extension deeper than a source extension as described in the present application and mentioned above. Rather, in one embodiment taught by Miller, a drain region is doped to achieve an drain underdiffusion length that is longer than a source underdiffusion length. See, Miller, Abstract, Figure 6, col. 2, lines 1-7 and lines 15-19 and col. 3, lines 9-17 and lines 60-62. The result is an increased gate-drain capacitance without providing a separate gate-drain capacitor and without requiring significant additional die area or critical mask alignment steps to form the capacitor. See, Miller, col. 1, lines 63-67 and col. 2, lines 1-10. Miller further teaches:

> Because of the increased drain underdiffusion, the gate may need to be lengthened, depending on the length of the underdiffusion, to maintain the required channel length between the self-aligned source and drain to avoid voltage breakdown of the silicon at the intended operating voltages.

See, Miller, col. 2, lines 21-25.

In addition, the portion of Miller cited by the Examiner to support this teaching states:

> The deep p+ drain 27 provides an increased length U_d of drain underdiffusion, which provides an increased gate-drain capacitance C_{gd}. The length of gates 28 are chosen so that the resulting channel length L_c, between sources 29 and drain 27 will be sufficient to sustain the operating voltages of the transistor without a voltage breakdown of the silicon.

See, Miller, col. 3, lines 60-67.

Accordingly, it is the length of the gates that is changed in order to correct for effects caused by the longer drain underdiffusion length used to create the increased gate-drain capacitance. There is no teaching or suggestion, however, that the longer drain underdiffusion length 1) improves the breakdown voltage characteristics of the silicon therefore limiting the effects of the short channel or "hot carrier effects; 2) provides substantial immunity to short channel effects; 2) reduces peak electric field in the channel region reduces the possibility of hot carrier injection into the gate oxide; and 4) provides higher drive current.

Because the has not established that the combination of Kadosh and Miller teaches the limitation that a drain extension is deeper than a source extension, and therefore has not established a prima facie case of obviousness, the Appellant's respectfully request reversal of the rejections of claims 18, 21-25, 28-35 and 37 over the combination of Kadosh and Miller.

(3) Appellants respectfully acknowledge the Examiner's agreement with the Appellant's arguments and the finding that Claim 36 includes patentable subject matter. The Examiner found that claim 36 should be objected to for the same reasons as claims 26 and 27.

CONCLUSION

In view of the foregoing, the Appellant submits that claims 18, 21-25 and 28-37 are not properly rejected under 35 USC § 103(a) as unpatentable over Kadosh in view of Miller and are patentable.

Accordingly, Appellant respectfully requests that the Board reverse all claim rejections and indicate that a Notice of Allowance respecting all pending claims should be issued.

Respectfully submitted,

Date 9/14/04 By Jean M. Tibbetts

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